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| **1475 SW Snively Ave**  **Chehalis, WA 98532** | **Cary D. Snyder** | **360-270-4848 Cell/Office**  **CarySnyder@ProtonMail.com** |

**SUMMARY**

Accomplished multi-domain technical resource who’s ready to come home to Chehalis! A resource with old-school commitment and dedication to duty from 8 years training in the US Air Force, where impossible was always possible with the right attitude. Comfortable wrenching on power train or chassis, or dealing with simple to complex mechanical-electrical subsystem or component modules. True value comes from being a down-to-earth team player who’s always willing to learn and share expertise as required. Expertise include:

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| * Autocad, media, mechanical-electronic design-tools & test   + Vehicle prototype & production system engineering and test   + Scripting languages/SW Debug   + Proprietary tool extensions, scrips, templates, etc.   + System/Sub-system Integration | * All aspects of electronic design and test to fully meet industry standards   + High-Speed interfaces, PCIe, USB, DDR3/4, TBT, Ethernet, system/chip   + Keen focus on 1st time production success including integration/volume manufacturing   + Chip/System power management & test | * Extensive Mechanical Design & Subsystem Project Management * Comprehensive system design, test, integration & manufacturing   + All types of CPUs & Microcontrollers   + Chassis, rack, & subsystem assembly   + Experienced in procurement |

## PROFESSIONAL EXPERIENCE

**Hardware Test Engineering Consultant –** Chehalis WASeptember 2018 – Current  
San Jose Bay Area, May 2010 to August 2018

Current full-time employee at UST Global with Contingent Worker assignment at Intel in Hillsboro OR. Test validation role with Intel x86 systems and subsystems including IO and media subsystems. Subject matter expertise (SME) covers x86 architecture (Haswell to Tiger Lake) and various embedded subsystem design topics. Fabrication duties include wireless subsystems and displays.

**Consulting Client Summary:** (HCL, eTeam, ERG, Triple Crown, Oxford, EJL Wireless, etc.)

**UST Global** – Hillsboro OR; Next Gen x86 Validation, Debug, DPMO Automation, Sensor Hub, Audio (2019)

**Astronics** – Kent WA; Airborne 150W PS/x86 Ctrl Design Project; Altium and PCB design (2018-2019)

**Keyssa** – Campbell CA/Portland WA startup; x86/Embedded USB+ Testing, tunneled through half-/full-duplex 60GHz links in pre- and post-ASIC peripheral system test engineer. SS+ RDK Test Engineering role. (2018)

**Sarokal / Intel & Others–***Infrastructure RRE/Radio Equipment* **CPRIe, 802.1 TSN,** Fronthaul test engineering, included 5G/4G infrastructure ASIC IP reverse-engineering of DDR3/DDR4, PCIe, ENet, & eCPRI interfaces.

**Microsoft 2x** – Xbox x86 Southbridge FPGA RDK/ASIC Test Engineer (PCIe, PM subsys USB, DDR & SATA)

**Broadcom** / **Intel** – Ultrabook RDK, Core M PCIe, M.2 Wi-Fi Module Test platform engineer (10 months)

**Broadcom** / **Apple** – New Intel Core-M Macbook system test / RDK and iPad Wi-Fi Module Test engineering   
**MoSys** / **HPE** – Dual DDR3 Memory IP Controller Debug and Bring-up as part of enterprise storage system.

**Maxim Semi** / **Microsoft** – USB x86 Test Engineer, Geo Semi WEBCAM RDK design test and validation

**Enlighted** – Embedded WiFi/Wireless Lighting Systems, System RDKs; FCC, UL, and Agency Compliance  
**Testronic Labs** – US Lab Manager for x86 USB, SATA, PCIe, DP testing JV with Agilent Pacific Northwest.

**Project Area Expertise with clients listed above:**

* Vehicle HUD and Infotainment prototyping projects; some hardened data-communication subsystem work
* USB SS/SS+ Compliance, Interoperability, Benchmark, and Power/Battery/Performance Testing (>5 yrs)
* Electro-Mechanical assembly and modeling design including aeronautical subsystem test design work.
* Teledyne/LeCroy Voyager/Ellisys EX350 USB SS+ Analyzer/Exercisers and Tests on multiple RDKs.
* LeCroy Kibra DDR3/4, SATA & PCIe Analyzers/Exercisers, and other BT/Bus Analyzers/Test Equipment
* Deep-dive bring-up with a hands-on test of Intel Core M mobile wireless architecture (See [*Haswell Rpt*](https://bytz.io/prod/doc.php?p=T4AZ5aa9557a6a4049.80118098&f=MPR_Article_HaswellULTIntegratesPCPlatform.pdf).).
* Considerable embedded product debug work covering x86 (Intel) and ARM processors, PCIe, USB, Ethernet, Networking (L1, L2/L3), SATA and Raid Controllers, including power subsystems. (> 24 months)
* Projects involved chip reverse engineering (RE); goal identify 4G IP structures and switching components.
* Evolved Core-M (m.2 PCIe) Wi-Fi test for Macbook/Ultrabook & WHQL compliance test. (> 10 months)
* Apply broad-based IP test & Validation skills to best manage risk to ensure timely success. (> 20 months)
* Windows x86, Android & iOS Testing (**Linux,** OSX, PC/Chrome) – Pre- & Post-ASIC Validation (5 years)
* Technical Reference Design Kit (RDK) product engineering and project management; USB, OTG, and US Test Lab work on PCIe and SATA reference design kits (RDKs on multiple projects)

*Technical Troubleshooter and IP Test Project schedule acceleration:*

* Dynamic clock and voltage scaling (DCVS) infrastructure IP analysis and test project(s).
* Hands-on device testing; Mini-PCIe/M.2 WiFi module bring-up thru WHQL compliance testing.
* Embedded test/validation to isolate and resolve unknown and non-replicated faults; DC-DC Converters and troubleshoot intermittent LDO design to meet UL924 in ceiling requirements.
* Supplemented ASIC design teams to id & resolve IP bugs to save >$50M for ASIC re-spins.
* System/Wireless Test Engineering at chip/module, board, and product levels w/FCC/UL Certs
* Extensive Customer Interface experience; wrote numerous App Notes & Product documentation.

**Mentor Graphics Corp. Embedded IP Specialist – San Jose, CA** May 2006 – May 2008

Took over four member Application engineering group single-handed (absorbed duties when hiring manager left with 3 weeks of starting assignment). Provided key factory apps support of key customers; Ericsson, Sony, ST Microelectronics, Delphi, AMD, ATI Tech, Texas Instruments, Samsung, ASUSTek, Microsoft, and others.

* Hands-On RDK development and validation testing for mobile cellular customers (WiFi/BT/Cellular).
* USB OTG REF RDK Platform Lead for HW, SW, and System testing. Headed USB Compliance Teams.
* Authored and published, participated in industry standards with HW/SW test/debug/validation platforms as a PCIe and USB-IF Engineer using Intel Linux/Embedded OS test sys in support of ASIC/SOC/Modules.

**VTM, Inc. Compliance Engineering/OTG USB Project Lead** Portland OR. August 2005 – April 2006

Performed various application engineering & staff roles for the USB Implementers Forum (USB-IF), Digital Living Alliance Network (DLNA), and other standards organizations. Managed the USB-IF OTG) Tester product from initial engineering validation to its formal worldwide release. Project support for Mentor Graphics and Intel.

**SemiView Inc. Semiconductor Industry Analyst** San Jose, CA July 2002 – August 2004

Primary duties included PCI Analyzer Products including PCIe Test and Validation. Additional duties included writing, editing, and consulting on FPGA semiconductor industry issues with a focus on emerging application specific trends. Consulting included FPGA Interface development, Hands-on FPGA/ASIC debug/validation.

**MDR/Microprocessor Report Senior Analyst, Editor San Jose CA** July 2000 – August 2002

Key processor, CPU, and SOC architectural analysist for the Microprocessor Report. Met and interacted with CTO- and Architect-level experts at Intel, ARM, IBM, Motorola, AMD, MIPS, and consulted with startups like Tensilica, ARC, Lexra, and others. Published over 30 articles including Xtensa and ARC design processes.

**Altera/Xilinx** **Senior IP Product Manager/Engineer San Jose CA** May 1996 – July 2000

Successfully defined and introduced Xilinx’s first PCI IP product when led to its IP business unit responsible for >$400M in annual sales. Manage the creation and release of IP dev platforms at Altera with a hands-on test development role. Authored and presented a paper at the DesignCon 2000.

**MILITARY SERVICE:**  Veteran U.S. Air Force, Honor Grad E-5, Staff Sergeant, 8 years, Honorable Discharge

**EDUCATION**:  
2010: Process Manufacturing coursework, Lower Columbia College, 58 semester hours, (3.79 GPA)  
-1995: BSEE Course work at San Jose State, University Berkley Extension, Emery Riddle Aeronautical Extension Europe, Park College at USAF facilities worldwide.  
AA Degree, Electronic Communication Systems: LACC/Community College of the Air Force

USAF: Honor Graduate Certificate. Microwave and RF theory, digital design, transmission lines, analog and power systems, engineering and installations management.  
  
Electrical Engineering BSEE Equivalency; >**280** credits from **13** Universities and Colleges worldwide  
  
**OTHER COURSEWORK and PROFESSIONAL TRAINING:**  SW Engineering at UCSC Extension, E-Business and Marketing Univ. of Phoenix, Honor Graduate from Technical and NCO Leadership and Safety Training in the US Air Force.

## Significant Project Accomplishment List

1. HUD subsystem prototype design projects; evolved into infotainment subsystems for ST Microelectronics
2. USB SS+/SS/HS Gold Device qualification testing projects (Embedded, Interchip, OTG+) over 15+ years.
3. Extensive Design Support of Failsafe RAID Control Storage System, & Network Switch connectivity, Fault-tolerant Power System, Electro-mechanical redesign to meet UL/Emissions FCC/TUV/susceptibility requirements.
4. PCB product design and redesign including cost reduction of 24-layer board and design-for-test (DFT) projects; work included EMI/EMC design changes resulting in meeting FCC Class B and EU Susceptibility tests.
5. Embedded product design work spans microcontroller and FPGA-based Nios/Microblaze soft-processor IP.
6. Worked on Cellular Infrastructure RE (reverse engineering) projects involved the identification of intellectual property (IP) and associated processing (reconfigurable and scalable) systems and subsystems. Powering up the equipment in various test configurations enabled different interface probing technics via open maintenance ports and various debug/manufacturing test and PCIe peripheral ports. Information collected and analyzed extracted essential and otherwise unavailable information to help guide further analysis and RE at the Si, PCB, modules and subsystems, boards, and system levels. This information enables the creation of vendor-specific software and system analysis on key hardware (HW: PCB & Si), subsystems, and radio systems.
7. Physical RE projects involved the identification of key system components and purchase of off-the-shelf equipment that were then torn-down and analyzed to extract essential and otherwise unavailable information into valued IP-related database that would be used to generate reports of all types at the Si, PCB, modules and subsystems, boards, and system levels. This information enabled the creation of vendor-specific SW, HW (PCB & Si), subsystem, and radio system architectures. Cost constraints typically restricted detailed internal FPGA analysis. However, how the FPGAs are integrated and implemented contributes to an overall understanding.
8. Organized and led a special 4G and Pre-5G Tutorial at DesignCON 2017 that included the special participation of 5G SMEs. Speakers include 5G technology experts Dr. Ghobad Heidari, President at GHB Intellect, Dr. Raghu Rao, Principal Architect at Xilinx Inc., and Dr. Yogendra Shah who is a Senior Director at Interdigital Communications. The tutorial and paper presentation with the information above is a rather substantial foundation for projects and positions at a number of Silicon Valley companies.
9. Defined and implemented **Broadcom**’s WiFi BU wide Core-M (**Intel**’s Haswell and Broadwell) test and validation program utilizing a modified ASUS Haswell-based Core-M Laptop. Created and oversaw the low volume (100 units) procurement, and significant modification and integration of tri-boot Core-M test systems. Identified and help eliminate an intermittent Si bug by coding a script that replicated a complex WHQL (Windows Hardware Quality Lab) sequence resulting in a Blue Screen Crash test method that eluded the (>50 member dev team) Si engineering for months (years).  My script would replicate the Crash on demand, allowing Chip designers to isolate and correct a serious bug. Contributed to the successful Macbook Air (**Apple**) launch in as a WiFi module test system developer.
10. Developed a comprehensive XBOX ONE production manufacturing test (>1000 units under test) for Microsoft that reduced a 60% test failure rate to less than 4% (<2% unknown failures). Captured an intermittent SATA subsystem bug by use of a PowerShell/Batch File Script that induced the failure on demand days prior to the final ASIC Spin (a refined script reproduce bug on demand to assist Si ASIC designers in isolating and eliminating a serious bug). The new XBOX synchronized test process was adopted company-wide (Redmond & MTV).
11. Conducted comprehensive USB Compliance testing on a Maxim Integrated new high-volume video camera Si product. Tests included correcting and improving Microsoft’s USB camera WHQL test process.
12. Oversaw and executed key priority high-volume manufacturing engineering role to develop, test, and execute FCC/UL Certification to stringent UL924 lighting control requirements and high-volume MFG test systems for Enlighted’s wireless lighting control systems. $2M joint venture with Agilent before losing funding.
13. Mentor Graphics—PCIe and USB IP Customer Support Role; solved major Si PCIe and USB IP design and integration bugs in STM’s automotive group’s subsystem used in multiple STMicro Si-based product. Debugged and solved a Mobile RDK flaw for TI, and a camera design for SONY, and a video subsystem for ATI and AMD.
14. Key PCIe Compliance Test Validation Role for the PCI Special Interest Group w/early PCIe (3GIO) testing.
15. Successful managed & accelerated USB-IF’s On-the-Go (OTG) test system as a hands-on test validation engineer.
16. Altera—As PCI IP group engineer isolated an intermittent design flaw that had previously gone undetected.
17. Xilinx—proposed and got approval for Xilinx’s first PCI IP Core and IP Validation environment as an employee. Project described as “best thing since sliced bread” & $100M profits in its 1st year! The successful execution of the project as a hands-on consultant gave birth to Xilinx’s IP Business Group that now averages $400M in sales.